Some Notes on the Performance of Wideband Sampling Receivers for EME Operations.

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Abstract

Wideband sampling receivers are gaining more and more attention from the amateur community. Unless the RF input signal is undersampled, such receivers usually cover only the HF frequency range up to about 50 MHz and need a suitable analog downconverter for EME operations at VHF or higher.
In this paper we present the fundamental equations which govern the behavior of a receiving system based on a analog downconverter which drives an HF sampling receiver, such as the Perseus SDR receiver I developed in 2007.
Numerical examples are provided for a VHF EME receiving system based on this architecture with particular emphasis on the tradeoff between the overall receiver blocking dynamic range and the system noise figure.

Wideband Sampling Receivers for Amateurs

A wideband sampling receiver relies on fast, high resolution A/D converters which sample a wideband portion of the RF spectrum and convert the analog input signal into the digital domain where the signal is then further processed by digital signal processing techniques.
A non-exhaustive list of this kind of receivers comprises models like the Matt Ettus - N2MJI's U.S.R.P., the RF-Space's SDR-14 and SDR-IQ, the HPSDR group's Mercury board, the Phil Covington – N8VB's QS1R board and the PERSEUS (Pretty Excellent Receiver for Software-Eager Unperceivable Signals) receiver I developed in 2007.
The basic block diagram of these receivers is almost identical and is depicted in Fig. 1

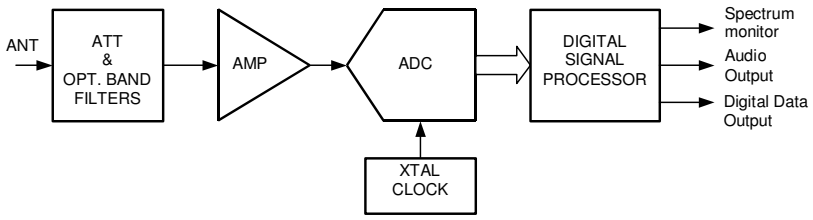

Fig. 1 – A typical block diagram of a wideband sampling receiver

The dynamic behavior of wideband sampling receivers is quite different from their analog counterparts. In analog receivers the blocking dynamic range is usually limited by the receiver preamplifier, by the 1st IF conversion mixer or by the 1st conversion LO phase noise.
In a well designed sampling receiver, instead, the blocking dynamic range (BDR) is essentially determined by the A/D converter full-scale voltage level.
If the composite input signal peaks exceed the A/D converter full-scale voltage level, a severe distortion is introduced.
If instead, the peaks are just below the A/D converter clipping level, then very low distortion is introduced by the A/D converter itself. In this case, the main distortion source is the front-end of the receiver, mainly the input preamplifier. This is generally the source of the intermodulation products. If these are within the received spectrum, even if they are not on top of your desired signal, they will mix with all the signals in the receiver's bandwidth and create more intermodulation and distortion. Furthermore, the total sum of all signals in the receiver bandwidth includes these undesired intermodulation products and the RMS sum of all the power in the receiver may cause the level to exceed the Blocking Dynamic Range (BDR) of the A/D. When the BDR is exceeded, the A/D will produce garbage signals

everywhere. Thus, as long as a sampling receiver is to be made "wideband", it is very important that the blocking dynamic range is carefully evaluated and possibly maximized.

In this paper, I will not address the topic of computing and optimizing the IMD3 (third order intermodulation products) dynamic range of a wideband sampling receiver. This particular issue requires a prior knowledge of the desired receiver noise figure, but given a particular A/D converter, there is a fundamental tradeoff between the overall receiver noise figure and its BDR.

The topics I will cover are:

a) given a desired receiver noise figure and a wideband A/D converter, how large can the BDR of a sampling receiver be made?
b) given a desired BDR, how small can the noise figure of a sampling receiver be made? And finally,
c) if I want to reduce my sampling receiver noise figure by 1dB, how large much would this reduce the BDR of the receiver?

Modeling a Sampling Receiver

Fig. 2 is an equivalent block diagram of a wideband sampling receiver useful for evaluating its noise figure. For the sake of simplicity, I have omitted some filters (i.e. the A/D converter anti-alias filter) which are required in sampling receivers. They can be represented as losses in the gain block.

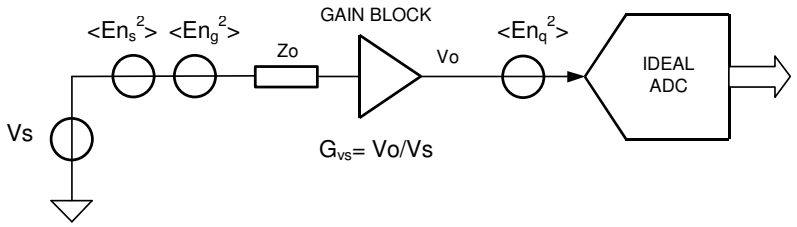

Fig. 2 – Wideband Sampling Receiver Model

In this model, the source generator is modeled by a voltage generator Vs with an output impedance of Zo Ohm. In series with the source there is a voltage noise generator $<En_s^2>$ which takes in account for the thermal noise of a signal source placed at the ambient temperature To. The noise voltage spectral density of the source generator is G_{ns} = 4kToZo V/sqrt(Hz), where k is the Boltzmann constant.
The gain block in front of the A/D converter is modeled by a noisy voltage amplifier and is characterized by two quantities, the voltage gain G_{vs} and by the noise figure F_g. We take in account the noise of the gain block by placing a voltage noise generator $<En_g^2>$, in series with the generator noise source, whose voltage spectral density is
$G_{ng} = 4(F_g-1)kToZo$, where F_g is the gain block noise figure, so that the total noise voltage spectral density at the input is exactly $G_{ni} = G_{ns} + G_{ng} = F_g$ kToZo, as required.
The A/D converter is modeled by an ideal A/D converter with a +/-V_{fs} full-scale voltage level. The A/D converter samples the voltage input at the rate Fc. To model the quantization noise, an equivalent noise generator $<En_q^2>$ is placed in series with the A/D input. Assuming that the A/D converter quantization noise is uniform across the frequency range from DC up to the Nyquist frequency F_n (half the sampling frequency Fc), the A/D converter noise voltage spectral density at the input of the converter is:

$$Gnq = \frac{V_{fs}^{\ 2}}{2SNR_{adc}F_n} \qquad (1)$$

where SNR_{adc} is the signal to noise ratio of the A/D converter.

When expressed in decibels, the ideal signal to noise ratio of an A/D converter is related to its bit resolution by the formula:

$$SNR = 1.76 + 6.02 \quad (dB) \tag{2}$$

where N is the number of bits which represent the sampled signal. In real high resolution converters this value is usually much lower.
It is worth noting that this model can be used to compute the noise figure and the blocking dynamic range of a sampling receiver even when the gain block is actually an analog down-converter, which is the actual way we will use this for EME. In this case, G_{vs} and F_g are the actual voltage gain and the noise figure of the down-converter. The voltage gain is a quantity seldom used to characterize a RF circuit. It is strictly related to both the power gain through the circuit input and also the output impedances.

Given the model in Fig. 2, the overall receiver noise figure can be easily computed referring to the receiver input the A/D converter quantization noise source $<En_q^2>$. The input referred A/D converter quantization noise voltage spectral density is simply $Gnqi = Gnq/ G_{vs}^2$. The total receiver total noise voltage spectral density is then:

$$Gni = 4F_g kToZo + Gnqi = 4kToZo(F_g + \frac{Gnq}{4G_{vs}^{\ 2} kToZo}) \tag{3}$$

and the overall receiver noise figure is:

$$Ftot = F_g + \frac{Gnq}{4G_{vs}^{\ 2} kToZo} \tag{4}$$

Now, since $G_{vs} = V_{fs} / V_{smax}$, where V_{smax} is the source input referred peak voltage which drives the A/D converter to full scale, and since $S_{max} = V_{smax}^2/(8Zo)$ is the available input signal power associated with the voltage V_{smax}, eq. (4) can be rewritten:

$$F_{tot} = F_g + \frac{2Gnq\, S_{\max}}{V_{fs}^{\ 2} kTo}, \tag{5}$$

and substituting eq. (1) in eq (5) we find:

$$F_{tot} = F_g + \frac{S_{\max}}{kTo} \frac{1}{SNR_{adc} F_n} \tag{6}$$

Noting that the receiver BDR referred to a 1 Hz bandwidth is simply:

$$BDR = \frac{S_{\max}}{F_{tot} kTo}, \tag{7}$$

eq. (6) can be rewritten

$$F_{tot} = F_g + F_{tot} \frac{BDR}{SNR_{adc} F_n} \tag{8}$$

or

$$F_{tot} = \frac{F_g}{1 - \frac{BDR}{SNR_{adc} F_n}} \tag{9}$$

Since F_{tot} is a positive quantity, from equation (9) we note that the receiver BDR cannot exceed the quantity $BDR_{adc}=SNR_{adc}\, F_n$, which is actually the A/D converter blocking dynamic range in a 1 Hz bandwidth.

Noise Figure vs. Blocking Dynamic Range

From eq. (9) we derive a very important fact about sampling receivers. Given the A/D converter specifications (its SNR and sampling frequency) and the noise figure F_g of its front-end gain block, there is a fundamental tradeoff between the overall receiver noise figure and its blocking dynamic range. If we need to improve the receiver noise figure, we have to do it at the expense of the receiver BDR and vice versa.
This fact can be explained in a simple manner noting that to reduce the receiver noise figure we have to make the preamplifier (gain block) noise be the dominant noise source. Since the ratio between the A/D converter noise spectral density and its full-scale power level is fixed, lowering the input referred A/D converter quantization noise below the preamplifier noise translates simply in a reduced full-scale power level at the receiver input.
If we define the quantity Q as:

$$Q = -10\log_{10}(1-\frac{BDR}{BDR_{adc}}) \tag{10}$$

From eq. (9) we have:

$$F_{tot}(dB) = F_g(dB) + Q \tag{11}$$

From eq. (11) we note that even if we were to use a noiseless gain block (F_g = 0dB), the overall receiver noise figure could become very large when attempting to maximize the sampling receiver BDR up to its theoretical limit BDR_{adc}. Since in general $F_g > 0$ dB, eq. (11) gives a lower limit to a wideband receiver noise figure, F_{min}, which is attainable when both the receiver BDR and the A/D converter BDR are given as independent parameters:

$$F_{tot}(dB) \geq F_{\min}(dB) = Q \tag{12}$$

In all practical cases the receiver noise figure will be just the sum of F_{min} and the gain block noise figure F_g.
If we define D as the A/D converter BDR degradation, that's to say the difference in dB between the A/D converter BDR and the actual receiver BDR:

$$D \equiv BDR_{adc}(dB) - BDR(dB) \tag{13}$$

Eq. (12) can be rewritten:

$$F_{\min} = -10\log_{10}(1-10^{-D/10}) \tag{14}$$

The theoretical receiver minimum noise figure F_{min} is plotted against the A/D converter BDR degradation D in Fig. 3.

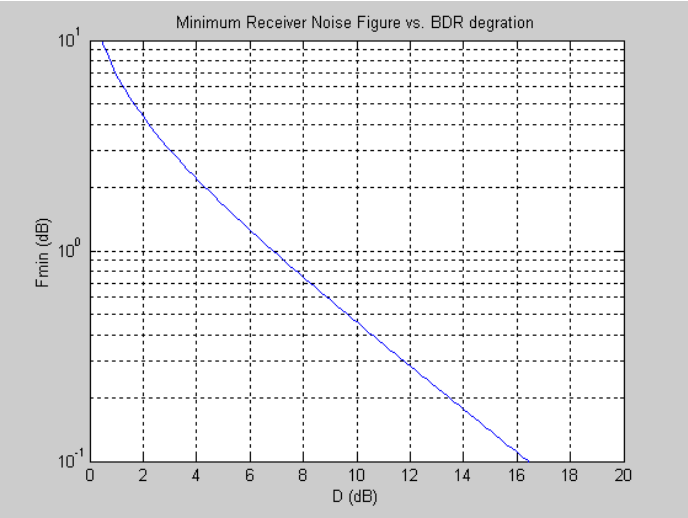

Fig. 3 – Minimum receiver noise figure as function of the A/D converter BDR degradation

The plot in Fig. 3 shows clearly that a low noise figure in a sampling receiver cannot be achieved unless a large degradation of the A/D converter blocking dynamic range is accepted.
The plot shows also that when a high receiver noise figure is tolerated (> 10 dB), as i.e. it usually happens in HF receivers, the A/D converter BDR degradation can be kept very small and usually within 1 dB.

It is worth noting that in a sampling receiver the tradeoff between the NF and the BDR does not depends upon the actual receiver architecture, i.e. whether the A/D converter is used in subsampling mode directly sampling a signal in the VHF frequency range, either an analog down-converter is placed in front of it and the A/D converter is used in its first Nyquist zone. The plot in Fig. 3 holds in any case.

Qualitatively the rule is very simple: when a low noise figure sampling receiver is needed, the receiver dominant noise source should be the noise of the gain block placed in front of the A/D converter. Unfortunately, in this case the dynamic range of the A/D converter is not limited by its quantization noise, but by the gain block noise which has to be much higher than the first, and thus the maximum SNR available at the A/D converter input (that's to say the system BDR) is much less than it would have been otherwise.

Fig. 3 gives also other important suggestions. How large BDR degradation can we expect when we try to reduce a VHF receiver noise figure from say 2.3 dB to 0.3 dB? If we ideally had a noiseless gain block the reply would be 12 – 4 = 8 dB (the BDR degradation is right the difference of the two D values, 12 and 4, corresponding to the given noise figures, 0.3 dB and 2.3 dB respectively). If instead we used a real gain block with even a low 0.3 dB noise figure, the BDR degradation would become very large and greater than about 14/15 dB! A loss which is more than two bits resolution of the A/D converter (see eq. (2)).

We can now reply to the questions we asked at the beginning of this paper:

Q. Given a desired receiver noise figure and a wideband A/D converter, how large can the BDR of a sampling receiver be made?
A. The BDR of a sampling receiver cannot exceed the BDR of a wideband A/D converter, nor the receiver noise figure can be less than the analog gain block placed in front of the A/D converter (it doesn't care if this block is simply an amplifier, like in subsampled receivers or an analog downconverter). Once the gain block noise figure F_g is known, subtract it from the desired receiver noise figure F_{tot}. This quantity is simply the noise figure F_{min} given in eq. (12).
Since $F_{min} = Q$, the A/D converter BDR degradation can be computed from eq. (11) and once the A/D converter is known it results:

$$BDR = BDR_{adc} - 10\log_{10}\left(\frac{1}{1-10^{\frac{Fg-Ftot}{10}}}\right) \qquad (15)$$

Example:
Desired receiver noise figure: Ftot = 1 dB
Gain block noise figure: Fg = 0.5 dB
Wideband A/D converter: LTC2206-14 (14 bit resolution, SNR = 76 dB @ 80 MS/s)

Solution:
From the A/D converter specification we compute:

$BDR_{adc} = SNR_{adc} + 10 \log_{10} (Fc/2) = 76 + 76 = 152$ dB/Hz

From eq. (15) it results:

BDR = 152 - 10log10(1/(1-10^((0.5 – 1)/10))) = 152 – 9.6 = 142.4 dB/Hz

Note that the A/D converter BDR degradation is as high as 9.6 dB! Note also that in a 500 Hz bandwidth (27 dB/Hz) the receiver BDR is 115.4 dB. Since the receiver sensitivity in the same bandwidth is No+Ftot+BW(dB) = -174 + 1+ 27 = -146 dBm, this receiver will clip at a –30.6 dBm input level (a modest S 9+42).

Q. Given a desired BDR, how small can the noise figure of a sampling receiver be made?
A. The receiver noise figure can't be made small than a minimum quantity which is directly related to the degradation of the A/D converter BDR we can tolerate. We also know that the receiver BDR is always less than that of the A/D converter. If we want a really low noise figure we 1) need a really low noise gain block (and this was already known) and 2) must accept a large degradation of the A/D converter BDR. Once a BDR degradation D has been chosen we can use eq. (14) (or alternatively the plot of Fig. 3) to compute the minimum receiver noise figure. The overall receiver noise figure will be the sum of this minimum noise figure plus the noise figure of the gain block.

Example:
Wideband A/D converter: LTC2206-14 (14 bit resolution, SNR = 76 dB @ 80 MS/s)
Desired receiver BDR: 120 dB in 500 Hz bandwidth

Solution:
From the A/D converter specification we know that BDR_{adc} = 152 dB/Hz (see previous question).
The desired receiver BDR referred to a 1 Hz bandwidth is : 120 + 27 = 147 dB/Hz and the actual BDR degradation D is 152 – 147 = 5 dB.
Using eq. (14) we compute the minimum receiver noise figure F_{min}:

$F_{min} = -10 \log_{10}(1-10^{(-5/10)}) = 1.65$ dB

The total receiver noise figure can't be lower than this value. If we use a gain block with a 0.35 dB noise figure, the total noise figure will be 2 dB.

Q. if I want to reduce my sampling receiver noise figure by 1dB, how large much would this reduce the BDR of the receiver?
A. If a reduction of the receiver noise figure is attained simply reducing the noise figure of the gain block placed in front of the A/D converter, without any other operation, the receiver BDR will actually increase by the same amount.
If instead the noise figure of the gain block can't be further reduced, the only way we have to improve the receiver noise figure is to increase the gain of the gain block itself so that the input referred quantization noise will be lower. The reduction of the BDR can be computed with the aid of eq.(14) once the receiver and the gain block noise figures are known.

Example:
Overall receiver noise figure: Ftot = 1.5 dB
Gain block noise figure: Fg = 0.2 dB

Desired receiver noise figure: Ftotd = 0.5 dB (original minus 1 dB)

Solution:
We assume that the noise figure of the gain block can't be further reduced.
From F_{tot} and F_g we compute $F_{min1} = F_{tot} - F_g$ = 1.3 dB. Looking at Fig. 3 we see that the BDR degradation is D_1=6 dB.
Since the new desired noise figure is 0.5 dB and Fg is not varied, we have to increase the gain of the A/D converter front-end so that the new F_{min} reduces to $(F_{totd} - F_g) = 0.5 - 0.2$ = 0.3 dB. Looking again at Fig. 3 we see that this F_{min} value corresponds to a new degradation factor D_2 = 12 dB.
The BDR reduction suffered to improve the receiver noise figure by 1 dB is thus $D_2 - D_1 = 12 - 6 = 6$ dB.

Conclusions

In this paper I have presented a model that relates some design parameters of wideband sampling receivers. The model reveals the connections between two important quantities, the receiver noise figure and its blocking dynamic range through simple but powerful equations which should help the reader understanding the fundamental tradeoffs needed to tune a wideband sampling receiver for best EME operations or for other demanding applications.

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73,
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